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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,169	09/12/2003	Norman W. Robson	FIS920030257US1	2168
32074	7590	01/26/2006	EXAMINER	
INTERNATIONAL BUSINESS MACHINES CORPORATION			DOAN, NGHIA M	
DEPT. 18G			ART UNIT	PAPER NUMBER
BLDG. 300-482			2825	
2070 ROUTE 52				
HOPEWELL JUNCTION, NY 12533			DATE MAILED: 01/26/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/605,169	ROBSON ET AL.
Examiner	Art Unit	
Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 12/19/2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-8 and 17-20 is/are rejected.
- 7) Claim(s) 9-16 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____.
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
Paper No(s)/Mail Date _____.	6) <input type="checkbox"/> Other: _____.

DETAILED ACTION

1. Responsive to communication application 10/605169 filed on 09/12/2003, claims 1-20 are pending.

Claims 1-3, 10-11, 17-20 have been amended.

2. Applicant's arguments with respect to claim1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claims 4-5, 12-13 and 20 are objected to because of the following informalities:

As to claim 4, line 1, before "integrated circuit" change "an" to "the" or "said".

As to claim 5, line 1, before "integrated circuit" change "an" to "the" or "said".

As to claim 12, line 1, before "integrated circuit" change "an" to "the" or "said".

As to claim 13, line 1, before "integrated circuit" change "an" to "the" or "said".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-8 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Voogel (US 6,281,696).**

6. **With respective to claims 1 and 20,** Voogel discloses a method of testing an integrated circuit structure comprising the steps of:

providing a semiconductor wafer containing a set of chip locations for forming a set of integrated circuits therein (fig. 2A; col. 4 ll. 64-67 and col. 5, ll. 1-9 – wafer 200, each location (IC region 140) include one or more transistor of IC 110, 300, which are provided multiple testing circuit--);

fabricating in said wafer a set of transistors specific to a particular integrated circuit in said chip locations (col. 1, ll. 30-35 and ll. 44-47 – fabricate a layout of basic cell, example transistors on the silicon wafer-- and fig. 3A –3D; col. 6, ll. 47-61 – fabricate IC 110 in location (IC region 140) on wafer 200 in figure 2A and 2B--);

before electrical completion of said integrated circuit (col. 3, ll. 25-30, col. 7, ll. 7-9 and ll. 25-31, and col. 10, ll. 18-21 – test earlier in the fabrication process--), connecting at least one subset (Fig. 3A elements [330A-330D] and [340A-340D], Fig. 3B elements [360A-360D] and [370A-370D], and Fig. 3C elements [410A-410D], [412A-412D], and [420A-420D]) of said set of transistors by a lithographic process in at least one chip location (col. 1, ll. 30-33 and ll. 47-51 – a layout consists of set of patterns, which are correspond to formation of transistor and interconnect structure, these patterns will be transferred on to silicon wafer using photolithographic (lithographic) --) in a test interconnect arrangement (fig. 3B, elements [380A-380D] and fig. 3C elements [320A-320D]) using interconnect levels close to semiconductor material in said semiconductor wafer (first metal layer) (col. 3, ll. 34-45, col. 5, ll. 20-35, col. 6, ll. 47-67, and col. 10, ll. 15-20 – the wafer is tested only up to metal 2 --); and

testing at least one parameter (voltage and current) of said subset of transistors (col. 9, ll. 19-23, ll. 40-43, and ll. 55-60 – testing or detecting a open and short circuit based on voltage source and current output--).

7. **With respective to claim 17**, Voogel discloses a method of testing an integrated circuit structure comprising the steps of:

providing a semiconductor wafer containing a set of chip locations for forming a set of integrated circuits therein (fig. 2A; col. 4 ll. 64-67 and col. 5, ll. 1-9 – wafer 200, each location (IC region 140) include one or more transistor of IC 110, 300, which are provided multiple testing circuit--);

fabricating in said wafer a set of transistors specific to a particular integrated circuit in said chip locations (col. 1, ll. 30-35 and ll. 44-47 – fabricate a layout of basic cell, example transistors on the silicon wafer-- and fig. 3A –3D; col. 6, ll. 47-61 – fabricate IC 110 in location (IC region 140) on wafer 200 in figure 2A and 2B--);

before electrical completion of said integrated circuit (col. 3, ll. 25-30, col. 7, ll. 7-9 and ll. 25-31, and col. 10, ll. 18-21 – test earlier in the fabrication process--), connecting at least one subset (Fig. 3A elements [330A-330D] and [340A-340D], Fig. 3B elements [360A-360D] and [370A-370D], and Fig. 3C elements [410A-410D], [412A-412D], and [420A-420D]) of said set of transistors by a lithographic process in at least one chip location (col. 1, ll. 30-33 and ll. 47-51 – a layout consists of set of patterns, which are correspond to formation of transistor and interconnect structure, these patterns will be transferred on to silicon wafer using photolithographic (lithographic) (photolithographic – the most common lithography technique in semiconductor

manufacturing--) and film formation process --) in a test interconnect arrangement (fig. 3B, elements [380A-380D] and fig. 3C elements [320A-320D]) using interconnect levels close to semiconductor material in said semiconductor wafer (first metal layer) (col. 3, ll. 34-45, col. 5, ll. 20-35, col. 6, ll. 47-67 and col. 10, ll. 15-20 – the wafer is tested only up to metal 2 --); and

testing at least one parameter (voltage and current) of said subset of transistors (col. 9, ll. 19-23, ll. 4043, and ll. 55-60 – testing or detecting a open and short circuit based on voltage source and current output--).

modifying a step in said integrated circuit process when a parameter of a said subset of transistors is out of specification (col. 3, ll. 16-20 and col. 8, ll. 46-50).

8. **With respective to claims 2 and 18**, Voogel discloses all the limitations as set forth claims, in which said test arrangement is constructed using only a first interconnect level (col. 3, ll. 34-38 and col. 5, ll. 30-35) above said set of transistors and the test is performed before further interconnect level are formed (col. 7, ll. 7-15 and ll. 25-31).

9. **With respective to claims 3 and 19**, Voogel discloses all the limitations as set forth claims, in which said test arrangement is constructed using both a first and second interconnect level above said set of transistors (col. 6, ll. 47-61 and col. 10, ll. 18-20 – up to metal level 2 --) and the test is performed before further interconnect level are formed (col. 7, ll. 7-15 and ll. 25-31).

10. **With respective to claims 4-6**, Voogel discloses all the limitations as set forth claims, in which said subset is a portion (sub-circuits module) (sub-block) of said integrated circuit (col. 1, ll. 20-27).

11. **With respective to claim 7**, Voogel discloses all the limitations as set forth claims, in which said subset comprises at least two sub-circuits module (sub-blocks) of said integrated circuit (col. 1, ll. 20-27).
12. **With respective to claim 8**, Voogel discloses a method according to claim 1, in which said test comprises providing an input test vector and recording output signals from said test structure (col. 1, ll. 27-30 and ll. 44-47).

Allowable Subject Matter

13. Claims 9-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
14. The following is a statement of reasons for the indication of allowable subject matter: the prior arts do not teach or fairly suggest limitation "a step of removing said test interconnect arrangement and depositing layer of said integrated circuit an interconnect in replacement thereof".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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